8. The device according to claim 5, wherein the third nitride semiconductor layer is in lattice matching to the first nitride semiconductor layer.

9. A nitride semiconductor device comprising:

a first nitride semiconductor layer formed of GaN;

a second nitride semiconductor layer formed on the first nitride semiconductor layer of $(In_TAl_{1-T})_SGa_{1-S}N$ $(0<S\leqq 1,\ 0<T\leqq 1)$;

a third nitride semiconductor layer formed on the second nitride semiconductor layer of $(In_YAl_{1-Y})_XGa_{1-X}N$ $(0<X\leqq 1,\ 0\leqq Y<1)$, an In composition ratio Y of the third nitride semiconductor layer being less that an In composition ratio T of the second nitride semiconductor layer;

a fourth nitride semiconductor layer formed on the third nitride semiconductor layer of GaN or In_PGa_QN $(0<P<1,\ 0<Q<1)$;

a fifth nitride semiconductor layer formed on the fourth nitride semiconductor layer of $In_UAl_WGa_VN$ $(0\leqq U<1,\ 0\leqq V<1,\ 0<W\leqq 1,\ U+V+W=1)$; and

an anode electrode and a cathode electrode formed on the fifth nitride semiconductor layer.

10. The device according to claim 9, wherein the In composition ratio T of the second nitride semiconductor layer is at least 0.3 and the In composition ratio Y of the third nitride semiconductor layer is 0.3 or less.

11. The device according to claim 9, wherein the third nitride semiconductor layer has a band gap smaller than that of the second nitride semiconductor layer.

12. The device according to claim 9, wherein the third nitride semiconductor layer is in lattice matching to the first nitride semiconductor layer.

13. A nitride semiconductor device comprising:

a first nitride semiconductor layer formed of GaN;

a second nitride semiconductor layer formed on the first nitride semiconductor layer of $(In_TAl_{1-T})_SGa_{1-S}N$ $(0<S\leqq 1,\ 0<T\leqq 1)$;

a third nitride semiconductor layer formed on the second nitride semiconductor layer of $(In_YAl_{1-Y})_XGa_{1-X}N$ $(0<X\leqq 1,\ 0\leqq Y<1)$, an In composition ratio Y of the third nitride semiconductor layer being less than an In composition ratio T of the second nitride semiconductor layer;

a fourth nitride semiconductor layer formed on the third nitride semiconductor layer of GaN or In_PGa_QN $(0<P<1,\ 0<Q<1)$;

a fifth nitride semiconductor layer formed of non-doped or n-type $Al_UGa_{1-U}N$ $(0<U\leqq 1)$;

a sixth nitride semiconductor layer formed on the fifth nitride semiconductor layer of non-doped or n-type nitride semiconductor;

a seventh nitride semiconductor layer formed on the sixth nitride semiconductor layer of $In_VAl_ZGa_{1-V-Z}N$ $(0<V\leqq 1,\ 0<Z<1)$;

a gate electrode formed in a recess structure having a bottom face which arrives at the sixth nitride semiconductor layer; and

a source electrode and a drain electrode formed on the fifth nitride semiconductor layer, the sixth nitride semiconductor layer, or the seventh nitride semiconductor layer so as to sandwich the gate electrode therebetween.

14. The device according to claim 13, wherein the In composition ratio T of the second nitride semiconductor layer is at least 0.3 and the In composition ratio Y of the third nitride semiconductor layer is 0.3 or less.

15. The device according to claim 13, wherein the third nitride semiconductor layer has a band gap smaller than that of the second nitride semiconductor layer.

16. The device according to claim 13, wherein the third nitride semiconductor layer is in lattice matching to the first nitride semiconductor.

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